PGT206 - Computer Architecture

This course is *Computer Architecture*, offered by the Department of Electronics Engineering Technology.

Get ModelSim 13.0.1 (Altera-Edition) setup. (MD5 checksum)

Announcements

[20160122] Welcome to PGT206 Computer Architecture!

Lecture Slides

- Lecture 0 - Course Introduction
- Lecture 1 - Foundations
- Lecture 2 - CPU Basics
- Lecture 3 - Processor Internals
- Lecture 4 - Enhancements
- Lecture 5 - CPU Externals
- Lecture 6 - CPU Design

Lab Notes

- Lab Work 1 - Introduction to Verilog and Digital Simulation (Slide 1) (Slide 2) (Slide 3)
- Lab Work 2 - Combinational Logic (Slide 4)
- Lab Work 3 - Sequential Logic (Slide 5)
- Lab Work 4 - State Machines (Slide 6)

Assignments

- Assignment 1:

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ASSIGNMENT 1
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Analyze the difference between a Booth Multiplier and a standard
partial product
multiplier. In addition to that, propose how a multiplier can be
built without
using shift logic (i.e. using only combinational logic). Choose
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any application
and justify which implementation is most suitable for that
particular need.

This is a group assignment, but marks will be evaluated
individually. Each student
needs to submit a separate SINGLE PAGE summary of your work
contribution.

ASSIGNMENT DUE: [W05/14] 15/03/2016 (Lecture Session)
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- Assignment 2:

  pgt206_201516s2_assign2.txt

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ASSIGNMENT 2
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Evaluate the complexity of a floating-point add/subtract OR a
floating-point
multiply/divide circuit. The evaluation must be based on an
included
block-level schematic diagram of the chosen circuit. A step-by-
step description
of how the circuit works (at clock signal level) must be provided.

This is a group assignment, but marks will be evaluated
individually.

ASSIGNMENT DUE: [W11/14] 03/05/2016 (Lecture Session)
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Lab Project

This is only for RY40 and RY44. Groups RY41 and RY43 will have similar requirements but details will be provided by your instructor.

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LAB PROJECT
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You are required to implement a soft-processor core (HDL-based) with
the
following minimum requirements:
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  - 8-bit microprocessor (instruction size, register size, etc.)
  - minimum 4 ALU functions (add,subtract,logical and, logical or)
  - a minimum of 8 registers
  - a basic instruction set to move data between registers and ALU

These requirements are necessary for submission and minimum grade B.
More functionality means better grades.

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ASSESSMENT REQUIREMENTS
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This is a group assignment. But marks will be evaluated individually,
taking
into account reviews from your group member. Each group needs to
prepare a
short demonstration (there will be a short FAQ session) and a simple
report
(not MORE than 10 pages) explaining your work. The report MUST include
a
section on the contributions of each team member.

PROJECT DUE: W14/14 25/05/2016@26/05/2016 (Lab Session)
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Course Synopsis

Official Synopsis - NOT written by me!

This course covers both the architectural and organizational aspects of computer systems. Architectural aspects of a system are defined as the features that are available to the operating system kernel such as the instruction set, data representations and peripheral interfaces. On the other hand, organizational aspects of a system are defined as the physical implementations that realize the features given for a system. These include the design of basic building blocks such as the ALU and the control unit, as well as the logic level interface of both internal and external units. This course expects the students to have a good fundamental on digital logic design (both combinatorial and sequential logic).

Course Outcome

1. Ability to interpret the theoretical aspects of computer organization and architecture
2. Ability to analyze existing design using theoretical knowledge and/or simulation tools
3. Ability to design and evaluate basic implementation of a microprocessor core based on given specifications

Course Assessment

	Examinations		Course Work		
Total Contribution	60%		40%		
Assessment	Mid-Term	Final Exam	Assignments	Lab Assessments	Lab Project
Contribution	20%	40%	10%	20%	10%

Course Syllabus

Week	Lecture	Laboratory	Notes

Week 01	• Fundamentals of Computer Architecture Slides
	  ◦ computer organization
	  ◦ computer architecure
	  ◦ number formats
	  ◦ integer arithmetic
		Lab Work 1	

Week 02	• Fundamentals of Computer Architecture (cont.)
	  ◦ integer arithmetic (cont.)
	  ◦ floating-point formats
	  ◦ floating-point processing
		Lab Work 1 (cont.)	

Week 03	• Computer Structure and Functions Slides
	  ◦ basic structures (registers, ALU, control unit, etc.)
	  ◦ basic functions (program storage, memory hierarchy, microcode, data transfer, etc.)
		Lab Work 2	**Assignment 1 Queue**

Week 04	• Computer Structure and Functions (cont.)
	  ◦ instruction handling (instruction set, fetch & decode, addressing)
	  ◦ performance measurement & assessment
		Lab Work 2 (cont.)	

Week 05	• Microprocessor Internals Slides
	  ◦ bus architecture
	  ◦ ALU revisited
	  ◦ memory management
		Lab Work 2 (cont.)	**Assignment 1 Due (5%)**

Week	Lecture	Laboratory	Notes

Week 06	• Microprocessor Internals (cont.)
	  ◦ cache management
	  ◦ floating-point arithmetic
		Lab Work 3	**Lab Assessment 1 (10%)**

Week 07	• Microprocessor Enhancements Slides ◦ pipeline structures	Lab Work 3 (cont.)	**Mid-term Examination (20%)**
Week 08	• Microprocessor Enhancements (cont.) ◦ superscalar architectures	Lab Work 3 (cont.)	**Assignment 2 Queue**
Week 09	• Microprocessor Externals Slides ◦ bus interfacing	Lab Work 4	

Week 10	• Microprocessor Externals (cont.)
	  ◦ real-time issues
	  ◦ interrupt handling
		Lab Work 4 (cont.)	**Assignment 2 Due (5%)**

Week 11	• Microprocessor Design Slides ◦ design specifications	Lab Project	**Lab Assessment 2 (10%)**
Week 12	• Microprocessor Design (cont.) ◦ TinyCPU implementation	Lab Project (cont.)	
Week 13	• Microprocessor Design (cont.) ◦ testing implementation	Lab Project (cont.)	
Week 14	• Microprocessor Design (cont.) ◦ advanced topics (e.g. embedded computing, distributed computing, etc.)	Lab Project (cont.)	**Lab Project Due (10%)**

Related Notes

IEEE Floating-Point Format

Concepts: 1 signed bit, biased exponents (instead of 2s-complement - midpoint as bias), leading-1 mantissa (except when E=0 ⇒ denormalized@subnormal value)

- 64-bit : 1 S , 11 E , 52 M

- 32-bit : 1 S , 8 E , 23 M
- 16-bit : 1 S , 5 E , 10 M (mine is 1-6-9: as reported in my thesis)

When E = (others ⇒ '1') : it's either INF (M=0) or NaN (M!=0)

For 8-bit exponent, the bias is at 127.

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Last update: **2026/02/08 03:46**