MY1CV: Education

Doctor of Philosophy (2024)

Ph.D. at UniMAP. Thesis submitted for evaluation in September 2023.

Thesis: Enhancing Post-Harvest *Harumanis* Mango Sorting Process using Fourier Descriptor on a Customizable Vision System

Abstract: The use of vision systems in agriculture has been found to be very beneficial and is quickly becoming somewhat of a necessity for a modern farming system. Various agriculture activities from crop monitoring to post-harvest processes like cleaning and sorting, can be improved tremendously with the help of vision systems. An architecture for a fully-customized vision system implementation that can be used to enhance the sorting process of *harumanis* mango is proposed. The proposed architecture is presented using generic design components that are not dependent on any hardware platform or software library. This makes it very easy to reimplement the system and to customize it to meet any required cost-performance ratio. A hardware-centric approach is used to obtain faster processing time. Using a Field-Programmable Gate Array (FPGA) as additional processing element to handle basic image processing tasks provide more time for the main processing element to focus on high level vision algorithms like object classifications and tracking. A couple of implementations have been tested on different FPGA devices and are found to be more than capable of executing basic image processing tasks at 30 frame-per-second (fps), which is the normal frame rate of most imaging device. This shows that is can easily be inserted in an existing system with minimal modifications, if any. An open-source image processing library written in C (my1imgpro) has been developed and used as the base code for the software side of the proposed architecture. A custom connected-component labelling (CCL) algorithm and a custom border-following algorithm have been developed on top of that library. Both algorithms, along with other software components, have been developed to implement the software components of the proposed architecture. Shaped-based classification of harumanis is also proposed as a new classification method instead of weight and size. Fourier Descriptors (FD) are used as the shape descriptor for harumanis mango classification. Using k-Means Clustering algorithm, all 306 contours that have been successfully detected are classified into 5 categories based on the 24-term FDs generated using centroid distance data. Further analysis shows that the 5 categories can be finalized into 3 fundamental categories (elongated, normal, odd). These can potentially be used as a new standard by which harumanis mango is sorted and graded for commercial market. A fully software-based system using the proposed architecture have been implemented on a desktop computer. The same code have also been successfully compiled and executed on a Raspberry Pi 3 platform, which enables the system to be highly portable. Using live camera feed, both implementations are able to classify all available harumanis mango images into the proposed grades. The processing rate of this implementation implies that the sorting process can be done for a volume of about 15-tonnes per day (assuming 8-hour of daily operation time of a single conveyor line). This indicates that a hardware-centric implementation should have a much better throughput than that.

Master of Science (2002)

M.Sc. by research at School of Electrical & Electronics Engineering, USM, specializing in

Microelectronics (Integrated Circuit Design). Thesis submitted for evaluation in January 2001.

Thesis: Implementation of a Cascadable MLP Neural Processor with Sliding Feeder Technique

Abstract: The design of a 16-bit floating-point MLP neural processor is presented. It utilizes the sliding feeder technique, which reduces the complexity of common neural network interconnections. A new 16-bit floating-point data format is also introduced here. Its ability to match its 32-bit counterpart in calculating the MLP with BEP algorithm is quite remarkable. In a test to train a network to solve the linearly inseparable XOR logical function, the neural processor has successfully converge to an acceptable solution at the same number of training required by a processor using the standard single-precision value. The leading zero detection method has also been improved to save area consumption. The standard MLP with BEP algorithm has been restructured into an object-oriented type of algorithm. This is due to the fact that, instead of having all the data (weight, bias and node values) in a single memory heap, they are distributed among all the cascaded neural processors. This also enables the processor to accommodate the insertion of the sliding feeder technique. Some useful computer software – Code Generator, FPC Tool, and Neural Processor Simulator - has also been developed. All in all, they have contributed to the design, simulation and validation of the neural processor. The serial transmission circuit is only based on simple shift logic. The speed of the serial transmission only affects the network when data needs to be fed forward or backward between the layers. This is because, for data sliding, data transmission is done while the time consuming floating-point calculation takes place.

Bachelor of Engineering (1997)

B.Eng. (Hons.) at School of Electrical & Electronics Engineering, USM, specializing in Microelectronics (Integrated Circuit Design).

Final Year Project: Title: “Design of an Integrated Circuit Implementing the Discrete Wavelet Transform”. A system-level design mainly as a proof of concept. Sub-circuit simulations of the arithmetic unit (transistor-level) was done using pspice (MicroSim).

Selected Courses: Integrated Circuit Design, Microprocessor Systems, Software Engineering.

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